2014

RENICE H1 Compact Flash Card Data Sheet

Renice Technology Co., Limited

2014-1-7

CATALOGUE

1. Introduction

1.1 Product Overview

Renice H1 Compact Flash comes with the industry standard Compact Flash form factor, provides both high performance and reliability, features great endurance in harsh environment such as low/high temperature, shock, vibration and interference. It can operate with a 3.3V/5V supply. A highly sophisticated Error Correction Code and a wear-leveling algorithm are also implemented. With these advantages and CF 4.1, CF 5.0 standard compatible,ATA-7 standard compatible in True-IDE mode, Fast ATA host-to-buffer transfer rates support PIO mode 6, MDMA mode 4, UDMA mode 6 in True-IDE mode.

Renice H1 Compact Flash is ideal storage option for embedded computing, industrial applications, network & communications, public security, military, aerospace, medical and automotive fields.

1.2 Feature

- **Interface standard:** IDE (50Pin)
- **Form factor:** 1.0 inch (42.8mmX36.4mmX3.3mm) L×W×H
- **Capacities:**

  MLC: 8GB, 16GB, 32GB, 64GB, 128GB

  SLC: 1GB, 2GB, 4GB, 8GB, 16GB, 32GB, 64GB
- **Input voltage:** 3.3V (±5%)
- **Temperature ranges:**

  Operation: 0 to +70℃ (Standard) -40 to +85℃(Industrial)

  Storage: -55 to +95℃
- **Intelligent features:**

  Built-in power fail detection for increased power fail robustness

  Data transfer rate to flash memories: up to 80 MByte/s

  Host data transfer rate in PIO mode 6 or MDMA mode 4 up to 25 MByte/sec

  Host data transfer rate in UDMA mode 6 up to 133 MByte/s

  Supports True-IDE mode

  On-chip ECC (BCH correcting 6, 8 or 24 bits) and CRC units

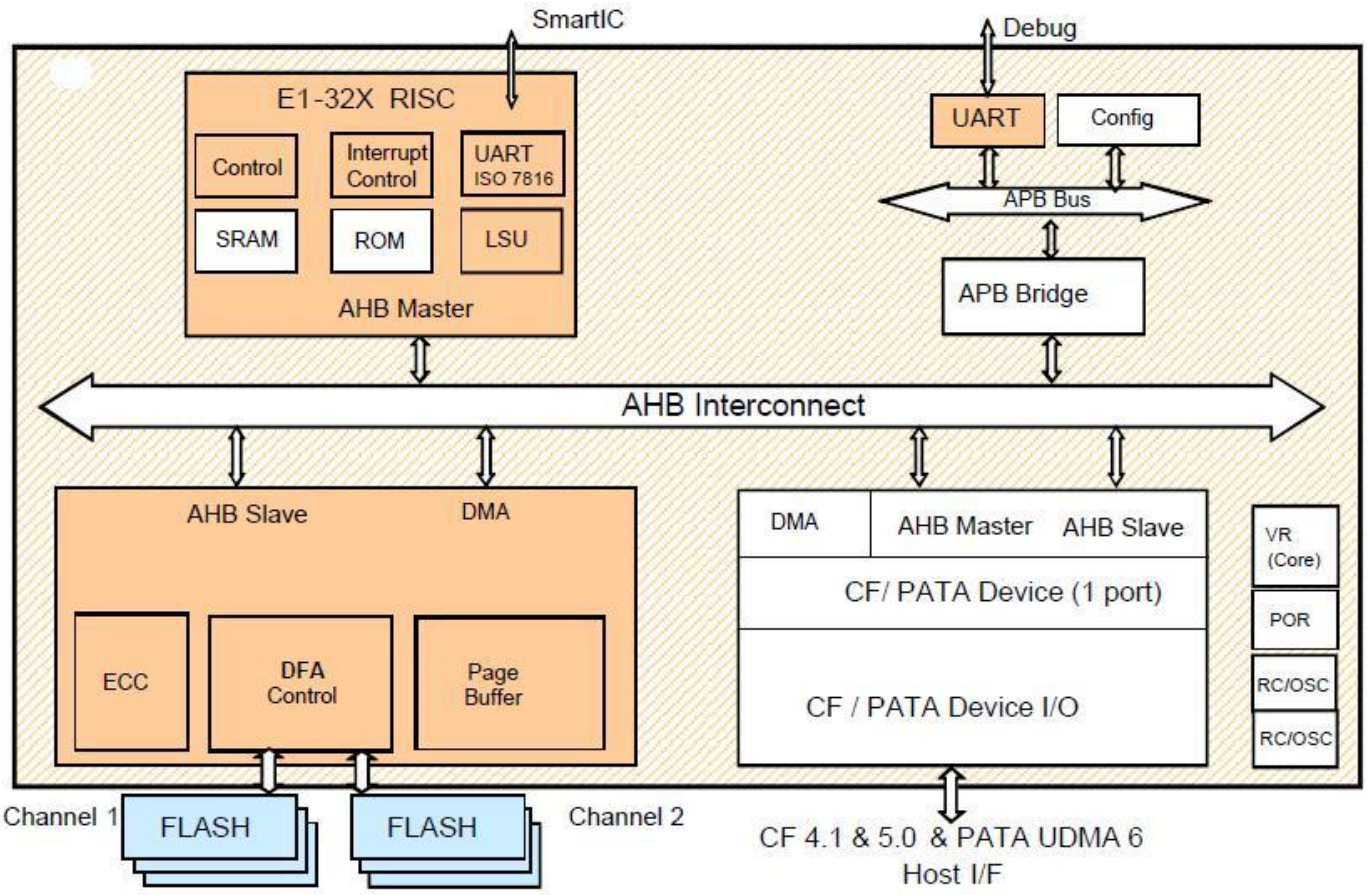
  Sophisticated software for wear leveling, SMART features, and read disturb handling

  Automatic power-down mode and sleep mode

  Direct flash access (DFA) mechanism

  Dual channel flash memory access
- **MTBF:** >3,000,000 Hours

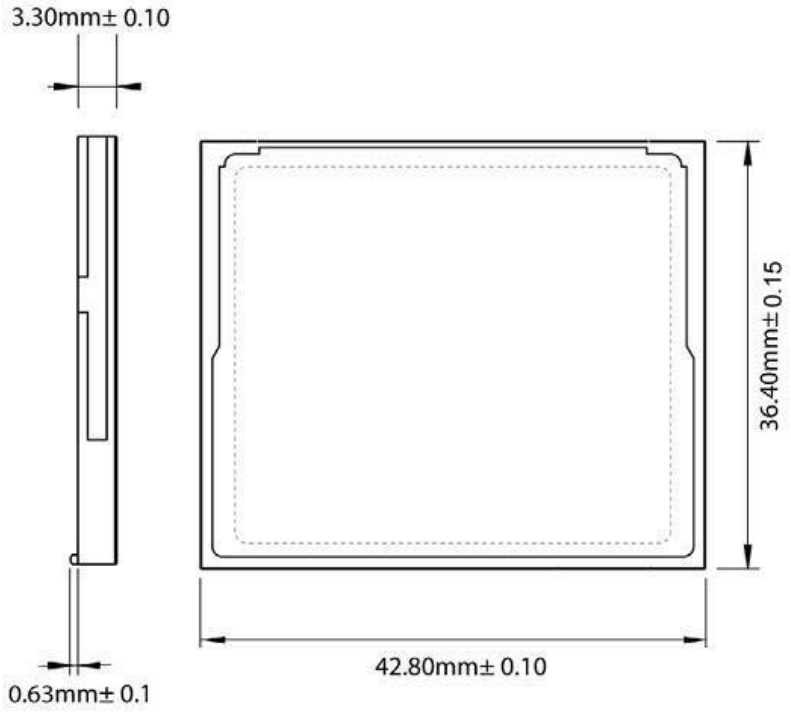
2. Functional Block Diagram



3. Product Specifications

3.1 Physical Specifications

Form factor		1.0 inch
Dimensions(mm)	Length	42.8±0.10
	Width	36.4±0.15
	Height	3.3±0.10
Weight		12±2g
Connector		50pin IDE



3.2 Host Interface

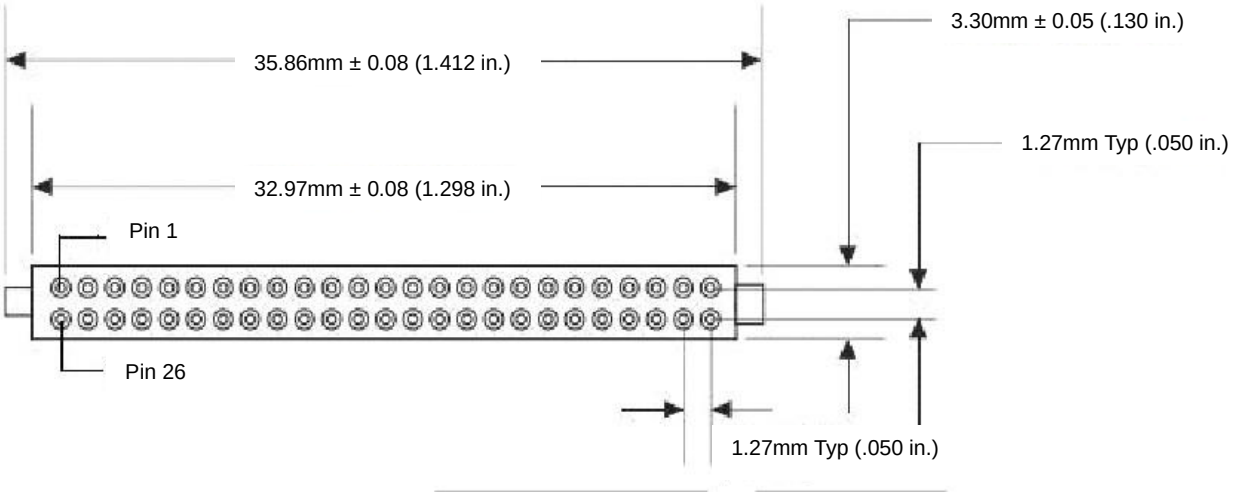
Fully compliant with CFA 4.1 and ATA-6 Standard

· ATA Transfer Modes:

- UDMA 0-6
- MWDMA 0-4
- PIO 0-6
- Error Correcting Code capable of correcting up to 8 bits in a 512 bytes sector, or up to 24 bits in a 1 Kbyte double sector
- Supports True IDE, PC Card Memory and I/O modes

4. Interface Description

4.1 Pin Assignment



4.2 Pin Description

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin No.	Name	I/O	Pin No.	Name	I/O	Pin No.	Name	I/O
1	GND		1	GND		1	GND	
2	D03	I/O	2	D03	I/O	2	D03	I/O
3	D04	I/O	3	D04	I/O	3	D04	I/O
4	D05	I/O	4	D05	I/O	4	D05	I/O
5	D06	I/O	5	D06	I/O	5	D06	I/O
6	D07	I/O	6	D07	I/O	6	D07	I/O
7	-CE1	I	7	-CE1	I	7	-CS0	I
8	A10	I	8	A10	I	8	A10[2]	I
9	-OE	I	9	-OE	I	9	-ATA SEL	I
10	A09	I	10	A09	I	10	A09[2]	I
11	A08	I	11	A08	I	11	A08[2]	I
12	A07	I	12	A07	I	12	A07[2]	I
13	VCC		13	VCC		13	VCC	
14	A06	I	14	A06	I	14	A06[2]	I
15	A05	I	15	A05	I	15	A05[2]	I
16	A04	I	16	A04	I	16	A04[2]	I
17	A03	I	17	A03	I	17	A03[2]	I
18	A02	I	18	A02	I	18	A02	I
19	A01	I	19	A01	I	19	A01	I
20	A00	I	20	A00	I	20	A00	I
21	D00	I/O	21	D00	I/O	21	D00	I/O
22	D01	I/O	22	D01	I/O	22	D01	I/O
23	D02	I/O	22	D02	I/O	22	D02	I/O
24	WP	O	24	-IOIS16	O	24	-IOCS16	O
25	-CD2	O	25	-CD2	O	25	-CD2	O
26	-CD1	O	26	-CD1	O	26	-CD1	O
27	D11[1]	I/O	27	D11[1]	I/O	27	D11[1]	I/O
28	D12[1]	I/O	28	D12[1]	I/O	28	D12[1]	I/O
29	D13[1]	I/O	29	D13[1]	I/O	29	D13[1]	I/O
30	D14[1]	I/O	30	D14[1]	I/O	30	D14[1]	I/O

PC Card Memory Mode			PC Card I/O Mode			True IDE Mode		
Pin No.	**Name**	**I/O**	**Pin No.**	**Name**	**I/O**	**Pin No.**	**Name**	**I/O**
31	D15[1]	I/O	31	D15[1]	I/O	31	D15[1]	I/O
32	-CE2[1]	I	32	-CE2[1]	I	32	-CS1[1]	I
33	-VS1	O	33	-VS1	O	33	-VS1	O
34	-IORD	I	34	-IORD	I	34	-IORD[7] HSTROBE[8] -HDMARDY[9]	I
35	-IOWR	I	35	-IOWR	I	35	-IOWR[7] STOP[8,9]	I
36	-WE	I	36	-WE	I	36	-WE[3]	I
37	READY	O	37	-IREQ	O	37	INTRQ	O
38	VCC		38	VCC		38	VCC	
39	-CSEL[5]	I	39	-CSEL[5]	I	39	-CSEL	I
40	-VS2	O	40	-VS2	O	40	-VS2	O
41	RESET	I	41	RESET	I	41	-RESET	I
42	-WAIT	O	42	-WAIT	O	42	IORDY[1] -DDMARDY[8] DSTROBE[9]	O
43	-INPACK	O	43	-INPACK	O	43	DMARQ	O
44	-REG	I	44	-REG	I	44	-DMACK[6]	I
45	BVD2	O	45	-SPKR	O	45	-DASP	I/O
46	BVD1	O	46	-STSCHG	O	46	-PDIAG	I/O
47	D08[1]	I/O	47	D08[1]	I/O	47	D08[1]	I/O
48	D09[1]	I/O	48	D09[1]	I/O	48	D09[1]	I/O
49	D10[1]	I/O	49	D10[1]	I/O	49	D10[1]	I/O
50	GND		50	GND		50	GND	

5. Power Specifications

5.1 Power Specification

Operating voltage: 3.3V (±5%)

5.2 Power Consumption (typical)

Operation (Read/Write):110mA/90mA (UDMA6)

Idle: 5mA

Sleep (Partial/Slumber):5mA/7mA (typ/max)

6. Reliability Specification

Item	Features	
Temperature	Operation	Standard: 0~70°C
		Industrial: -40~+85°C
	Storage	-55~+95°C
Humidity	5-95%	
Vibration	10Hz-2000Hz, 16.4 G (X, Y, Z axis, 1 hour /axis)	
Shock	Peak Acceleration: 1,500 G, 0.5ms(Half-sine wave, ±X,±Y,±Z axis, 1 time/axis) Peak Acceleration: 50 G, 11ms(Half-sine wave, ±X,±Y,±Z axis, 3 times/axis)	

6.1 Wear-leveling

Renice H1 Compact Flash supports both static and dynamic wear-leveling; these two algorithms guarantee all type of flash memory at same level of erase cycles to improve lifetime limitation of NAND based storage.

6.2 Endurance

Data retention: >10 years (@25C)

Read endurance: JESD47 compliant

6.3 H/W ECC and EDC for NAND Flash

Error Correcting Code capable of correcting up to 8 bits in a 512 bytes sector, or up to 24 bits in a 1 Kbyte double sector.

6.4 MTBF

MTBF (Mean Time between Failures) of Renice SSD: >3,000,000 hours

6.5 Over voltage and inrush current protection

The over voltage and inrush current protection mechanism of Renice H1 Compact Flash is to deploy a protect circuitry on Device Power In. Once the current or voltage is exceeded, it will be pulled down to the normal value in very short time to protect the drive.

7. Electrical Characteristics

7.1 DC Characteristics

Absolute Maximum Ratings

Supply voltage VDDS, VDDS2: -0.3V to 3.9V

Supply voltage VDDC: -0.3V to 3.0V

Voltage on the CF pins with respect to ground: -0.3V to 6.7V

Voltage on other pins with respect to ground: -0.3V to VDDS2 + 0.3V

Storage Temperature: -40°C to +125°C

D.C. Parameters

Supply Voltage VDDS, VDDS2: 3.3V ± 0.30V

Supply Voltage VDDC: 1.5V ± 0.10V

Temperature (ambient): 0°C to +70°C (commercial)
-40°C to +85°C (industrial)

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input LOW Voltage	-03	0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{DDS2} +0.3	V	
V_{IH}	Input HIGH Voltage, CF pins	2.0	5.5	V	
V_{OL}	Output LOW Voltage		0.4	V	At 4mA (12mA for DASP)
V_{OH}	Output HIGH Voltage	2.4		V	At 4mA
I_{CC}	Operating Current (VDDC) Sleep mode Operating, 60 MHz Operating, 80MHz		 … … …	 mA mA mA	 Typical … mA Typical … mA Typical … mA
I_{LI}	Input Leakage Current		± 10	µA	if not pull-up/pull-down
I_{LO}	Output Leakage Current		± 10	µA	If not pull-up/pull-down
$C_{I/O}$	Input/output Capacitance		10	pF	

Voltage Regulator Parameters

Output voltage: 1.5V ± 5%

Output current (max): 300mA

7.2 AC Characteristics

The AC Characteristics reference the timing diagrams of the Compact Flash Specification Revision 4.1 and the symbols in these timing diagrams. The AC characteristics are valid for a supply voltage of 3.3V ± 0.3V.

7.2.1. Attribute Memory Read and Write Characteristics

Symbol	Parameter	Min	Max	Units
tc(R)	Read cycle time	250		ns
ta(A)	Address access time		250	ns
ta(CE)	Card Enable access time		250	ns
ta(OE)	Output Enable access time		125	ns
tdis(CE)	Output disable time from CE		100	ns
tdis(OE)	Output disable time from OE		100	ns
ten(CE)	Output enable time from CE	5		ns
ten(OE)	Output enable time from OE	5		ns
tv(A)	Data valid time from address change	0		ns
tsu(A)	Address setup time	30		ns
tc(W)	Write cycle time	250		ns
tw(WE)	Write pulse time	150		ns
trec(WE)	Address hold time from WE	30		ns
tsu(D-WEH)	Data setup time for WE	80		ns
th(D)	Data hold time	30		ns

7.2.2. Common Memory Read and Write Characteristics

Symbol	Parameter	Min	Max	Units
tc	Cycle time	80		ns
ta(OE)	Output Enable access time		45	ns
tdis(OE)	Output disable time from OE		45	ns
tsu(A)	Address setup time	10		ns
th(A)	Address hold time	10		ns
tsu(CE)	Card Enable setup time	0		ns
th(CE)	Card Enable hold time	10		ns
tw(WE)	Write pulse time	55		ns
tsu(A)	Address setup time for WE	10		ns
tsu(CE)	Card Enable setup time for WE	0		ns
tsu(D-WEH)	Data setup time for WE	30		ns
th(D)	Data hold time	10		ns
trec(WE)	Write recovery time	15		ns

7.2.3. I/O Access Read and Write Characteristics

Symbol	Parameter	Min	Max	Units
td (IORD)	Data delay after IORD		45	ns
th (IORD)	Data hold following IORD	5		ns
tw (IORD)	IORD pulse width	55		ns
tsuA (IORD)	Address setup time for IORD	15		ns
thA (IORD)	Address hold time from IORD	10		ns
tsuCE (IORD)	Card Enable setup time for IORD	5		ns
thCE (IORD)	Card Enable hold time from IORD	10		ns
tsuREG (IORD)	REG setup time for IORD	5		ns
thREG (IORD)	REG hold time from IORD	0		ns
tdfINPACK (IORD)	INPACK delay falling from IORD	0	45	ns
tdrINPACK (IORD)	INPACK delay rising from IORD		45	ns
tdfIOIS16 (ADR)	IOIS16 delay falling from address		35	ns
tdrIOIS16 (ADR)	IOIS16 delay rising from address		35	ns
tsu (IOWR)	Data setup time for IOWR	15		ns
th (IOWR)	Data hold time from IOWR	5		ns
tw (IOWR)	IOWR pulse width	55		ns
tsuA (IOWR)	Address setup time for IOWR	15		ns
thA (IOWR)	Address hold time from IOWR	10		ns
tsuCE (IOWR)	Card Enable setup time for IOWR	5		ns
thCE (IOWR)	Card Enable setup time for IOWR	10		ns
tsuREG (IOWR)	REG setup time for IOWR	5		ns
thREG (IOWR)	REG hold time from IOWR	0		ns

7.2.4. True-IDE PIO Mode Read and Write Characteristics

Symbol	Parameter	Min	Max	Units
t0	Cycle time	80		ns
t1	Address setup time for IORD/IOWR	10		ns
t9	Address hold time from IORD/IOWR	10		ns
t2	IORD/IOWR pulse width	55		ns
t2i	IORD/IOWR recovery time	20		ns
t5	Data setup time for IORD	10		ns
t6	Data hold following IORD	5		ns
t6z	Output disable time from IORD		20	ns
t3	Data setup time for IOWR	15		ns
t4	Data hold following IOWR	5		ns

7.2.5. True-IDE MDMA Mode Read and Write Characteristics

Symbol	Parameter	Min	Max	Units
tO	Cycle time	80		ns
tD	IORD/IOWR pulse width	55		ns
tE	IORD data access		45	ns
tF	Data hold following IORD	5		ns
tG	Data setup time for IORD/IOWR	10		ns
tH	Data hold following IOWR	5		ns
tI	DMACK setup time for IORD/IOWR	0		ns
tJ	DMACK hold following IORD/IOWR	5		ns
tKR, tKW	IORD/IOWR recovery time	20		ns
tLR, tLW	IORD/IOWR to DMARQ delay		35	ns
tM	CS0, CS1 setup for IORD/IOWR	5		ns
tN	CS0, CS1 hold following IORD/IOWR	10		ns
tZ	Output disable time from DMACK		25	ns

7.2.6. True-IDE UDMA Mode Read and Write Characteristics

The interface timing in the True-IDE UDMA modes is not only depending on the interface hardware, but also on the correct setup of the UDMA registers in the firmware, according to the UDMA transfer mode selected by the host. With a correct register setup, the interface timing complies to the UDMA Mode 0 to Mode 6 timing specifications of the CF Specification Revision 4.1, and to the UDMA Mode 0 to Mode 6 timing specifications of the ATA/ATAPI-7 Standard.

7.2.7. Flash Memory Interface Characteristics

The AC Characteristics for the flash memory interface are based on the H1 processor clock cycle time tCPU. The table lists the flash memory interface timing based on the tCPU value, valid for a load of not more than 45pF on the flash interface pins.

Symbol	Parameter	Type	Value	Units
tCLS, tALS	CLE/ALE setup time, WE rising	(min)	tCPU*1.5-6ns	ns
tCLS, tALS	CLE/ALE setup time, WE falling	(min)	tCPU*0.5-2ns	ns
tCLH	CLE/ALE hold time	(min)	tCPU*0.5-1.2ns	ns
tCS	CE setup time, WE rising	(min)	tCPU*2.5-6ns	ns
tCS	CE setup time, WE falling	(min)	tCPU*1.5-6ns	ns
tCH	CE hold time	(min)	tCPU*1.5-6ns	ns
tDS	Data Setup time	(min)	tCPU*1.5-6.5ns	ns
tDH	Data hold time	(min)	tCPU*0.5-1.2ns	ns
tWP	WE pulse width	(typ)	tCPU	ns
tWC	Write cycle time	(typ)	tCPU*2	ns
tWH	WE high hold time	(min)	tCPU-3ns	ns
tRP	RE pulse width	(typ)	tCPU	ns
tRC	Read cycle time	(typ)	tCPU*2	ns
tREA	RE access time	(max)	tCPU*2-5ns	ns
tREH	RE high hold time	(min)	tCPU-3ns	ns
tWHR	WE high to RE low	(typ)	tCPU*6	ns

8. Software Interface

8.1 CF ATA Command Set

The following table lists the ATA commands that are supported

No.	Command name	Code	FR	SC	SN	CY	DR	HD	LBA
1	Check power mode	E5h, 98h	—	—	—	—	Y	—	—
2	Data Set Management	06h	—	Y	—	—	Y	—	—
3	Download Microcode	92h	Y	Y	Y	—	Y	—	—
4	Erase sector (s)	C0h	—	Y	Y	Y	Y	Y	Y
5	Execute drive diagnostic	90h	—	—	—	—	—	—	—
6	Flush Cache	E7h	—	—	—	—	Y	—	—
7	Flush Cache Ext	EAh	—	—	—	—	Y	—	—
8	Format track	50h	—	Y	—	Y	Y	Y	Y
9	Identify Device	ECh	—	—	—	—	Y	—	—
10	Idle	E3h, 97h	—	Y	—	—	Y	—	—
11	Idle immediate	E1h, 95h	—	—	—	—	Y	—	—
12	Initialize drive parameters	91h	—	Y	—	—	Y	Y	—
13	Media Lock	DEh	—	—	—	—	Y	—	—
14	Media Unlock	DFh	—	—	—	—	Y	—	—
15	NOP	00h	—	—	—	—	Y	—	—
16	Read buffer	E4h	—	—	—	—	Y	—	—
17	Read DMA	C8h, C9h	—	Y	Y	Y	Y	Y	Y
18	Read DMA Ext	25h	—	Y	Y	Y	Y	Y	Y
19	Read Log Ext	2Fh	—	Y	Y	Y	Y	—	Y
20	Read Multiple	C4h	—	Y	Y	Y	Y	Y	Y
21	Read Multiple Ext	29h	—	Y	Y	Y	Y	Y	Y
22	Read sector (s)	20h, 21h	—	Y	Y	Y	Y	Y	Y
23	Read sector (s) Ext	24h	—	Y	Y	Y	Y	Y	Y
24	Read verify sector (s)	40h	—	Y	Y	Y	Y	Y	Y
25	Read verify sector (s) Ext	42h	—	Y	Y	Y	Y	Y	Y
26	Recalibrate	1Xh	—	—	—	—	Y	—	—

No.	Command name	Code	FR	SC	SN	CY	DR	HD	LBA
27	Request sense	03h	—	—	—	—	Y	—	—
28	Sanitize Device	B4h	—	—	—	—	Y	—	—
29	Security Disable Password	F6h	—	—	—	—	Y	—	—
30	Security Erase Prepare	F3h	—	—	—	—	Y	—	—
31	Security Erase Unit	F4h	—	—	—	—	Y	—	—
32	Security Freeze Lock	F5h	—	—	—	—	Y	—	—
33	Security Set Password	F1h	—	—	—	—	Y	—	—
34	Security Unlock	F2h	—	—	—	—	Y	Y	—
35	Seek	7Xh	—	—	Y	Y	Y	Y	Y
36	Set features	EFh	Y	—	—	—	Y	—	—
37	Set multiple mode	C6h	—	Y	—	—	Y	—	—
38	Set sleep mode	E6h, 99h	—	—	—	—	Y	—	—
39	SMART	B0h	Y	Y	—	Y	Y	—	—
40	Stand by	E2h, 96h	—	Y	—	—	Y	—	—
41	Stand by immediate	E0h, 94h	—	—	—	—	Y	—	—
42	Translate sector	87h	—	Y	Y	Y	Y	Y	Y
43	Write buffer	E8h	—	—	—	—	Y	—	—
44	Write DMA	CAh, CBh	—	Y	Y	Y	Y	Y	Y
45	Write DMA Ext	35h	—	Y	Y	Y	Y	Y	Y
46	Write Log Ext	3Fh	—	Y	Y	Y	Y	—	Y
47	Write Multiple	C5h	—	Y	Y	Y	Y	Y	Y
48	Write Multiple Ext	39h	—	Y	Y	Y	Y	Y	Y
49	Write Multiple w/o erase	CDh	—	Y	Y	Y	Y	Y	Y
50	Write sector (s)	30h, 31h	—	Y	Y	Y	Y	Y	Y
51	Write sector (s) Ext	34h	—	Y	Y	Y	Y	Y	Y
52	Write sector (s) w/o erase	38h	—	Y	Y	Y	Y	Y	Y
53	Write verify	3Ch	—	Y	Y	Y	Y	Y	Y

Notes: FR: Feature Register
SC: Sector Count register
SN: Sector Number register
CY: Cylinder Low/High register
DR: Drive bit of Drive/Head register
HD: Head No. (0 to 15) of Drive/Head register
Y: Used for the command
—: Not used for the command

8. 2 SMART Command

The H1 supports the following SMART commands, determined by the Feature Register value.

Value	Command
D0h	SMART Read Data
D1h	SMART Read Attribute Thresholds
D2h	SMART Enable/Disable Attribute Autosave
D5h	SMART Read Log
D6h	SMART Write Log
D8h	SMART Enable Operations
D9h	SMART Disable Operations
DAh	SMART Return Status
E0h	SMART Read Remap Data
E1h	SMARR Read Wear Level Data

SMART commands with Feature Register values not mentioned in the above table are not Supported, and will be aborted.

8.2.1. SMART Enable Operations

COMMAND CODE B0h with a Feature Register value of D8h
PROTOCOL Non-data.
INPUTS

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS none required.
ERROR OUTPUTS aborted if the signature in the Cylinder registers is invalid.
DESCRIPTION this command enables access to the SMART capabilities of the H1 firmware. The state of SMART (enabled or disabled) is preserved across power cycles.

8.2.2. SMART Disable Operations

COMMAND CODE B0h with a Feature Register value of D9h
PROTOCOL Non-data. INPUTS

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS None required.
ERROR OUTPUTS Aborted if either the signature in the Cylinder registers is invalid,
or if SMART is not enabled.
DESCRIPTION This command disables access to the SMART capabilities of theH1 firmware.
The state of SMART (enabled or disabled) is preserved across power cycles.

8.2.3. SMART Enable/Disable Attribute Autosave

COMMAND CODE B0h with a Feature Register value of D2h
PROTOCOL Non-data.
INPUTS

Register	7	6	5	4	3	2	1	0
Feature	D2h							
Sector Count	00h or F1h							
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

8.2.4. SMART Read Data

COMMAND CODE B0h with a Feature Register value of D0h
PROTOCOL PIO data in. INPUTS

Register	7	6	5	4	3	2	1	0
Feature	D0h							
Sector Count								
Sector Number								
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	1	1	D				
Command	B0h							

NORMAL OUTPUTS None required.
ERROR OUTPUTS Aborted if either the signature in the Cylinder registers is invalid or if SMART is not enabled.

8.2.5. SMART data structure

This command returns one sector of SMART data. The data structure returned is:

Offset	Value	Description
0..1	0010h	SMART structure version
2..361		Attribute entries 1 to 30 (12 bytes each)
362	00h	Off-line data collection status (no off-line data collection)
363	00h	Self-test execution status byte (self-test completed)
364..365	0000h	Total time to complete off-line data collection
366	00h	—
367	00h	Off-line data collection capability (no off-line data collection)
368..369	0003h	SMART capabilities
370	00h	Error logging capability (no error logging)
371	00h	—
372	00h	Short self-test routine recommended polling time
373	00h	Extended self-test routine recommended polling time
374..385	00h	Reserved
386..387	0004h	SMART Structure Version
388..391		Firmware "Commit" counter
392..395		Firmware Wear Level Threshold
396		Global Wear Leveling active
397		Global Bad Block Management active
398..401		Average Flash Block Erase Count
402..405		Number of Flash Blocks involved into the Wear Leveling
406..409		Number of total ECC errors during firmware initialization
410..413		Number of correctable ECC errors during firmware initialization
414..510	00h	—
511		Data structure checksum

8.3 ID Table Information

8.3.1 ID Table Information of True IDE Mode

The following table lists the information returned by the Identify Device ATA command in the True-IDE mode, assuming that the –ext option has been used during the preformat.

Word Address	Default Value	Bytes	Data Field Type Information
0	045AH	2	General configuration bit-significant information (-id2)
1	XXXXH	2	Default number of cylinders
2	0000H	2	Reserved
3	00XXH	2	Default number of heads
4	0000H	2	Number of unformatted bytes per track
5	0200H	2	Number of unformatted bytes per sector
6	XXXXH	2	Default number of sectors per track
7 to 8	XXXXH	4	Number of sectors per card
9	0000H	2	Reserved
10 to 19	XXXXH	20	Serial Number (20 ASCII characters)
20	0002H	2	Buffer type (dual-ported multi-sector)
21	0001H	2	Buffer size in 512 byte increments
22	0004H	2	# ECC bytes passed on Read/Write Long Commands
23 to 26	XXXXH	8	Firmware revision (8 ASCII characters)
27 to 46	XXXXH	40	Model Number (40 ASCII characters)
47	8001H	2	Maximum 1 sector on Read/Write Multiple command
48	0000H	2	Double Word not supported
49	0F00H	2	Capabilities: DMA, LBA, IORDY supported
50	4001H	2	Capabilities: device specific standby timer minimum

Word Address	Default Value	Bytes	Data Field Type Information
51	0200H	2	PIO data transfer cycle timing mode 2
52	0000H	2	DMA data transfer cycle timing mode not supported
53	0007H	2	Data Fields 54 to 58, 64 to 70 and 88 are valid
54	XXXXH	2	Number of current logical cylinders
55	XXXXH	2	Number of current logical heads
56	XXXXH	2	Number of current logical sectors per track
57 to 58	XXXXH	4	Current Capacity in sectors
59	010XH	2	Multiple sector setting is valid
60 to 61	XXXXH	4	Total number of sectors addressable in LBA Mode
62	0000H	2	Single Word DMA transfer not implemented
63	0X0XH	2	Multi Word DMA transfer mode, -mdma preformat option
64	0003H	2	Advanced PIO Modes: modes 3 and 4 supported
65	0078H	2	Minimum Multi Word DMA cycle time, 0 if no MDMA
66	0078H	2	Recommended Multi Word DMA cycle time, 0 if no MDMA
67	0078H	2	Minimum PIO cycle time without flow control
68	0078H	2	Minimum PIO cycle time with flow control
69 to 79	0000H	22	Reserved
80	01E0H	2	Major version number, ATA-5 to ATA-8 support
81	0000H	2	Minor version number, not reported
82	702BH	2	Command set: NOP, READ BUFFER, WRITE BUFFER, volatile write cache, power management feature set, Security Mode feature set, SMART feature set
83	7405H	2	Command set: FLUSH CACHE, FLUSH CACHE EXT, LBA48, CFA feature set, DOWNLOAD MICROCODE
84	4020H	2	Command set/feature supported extension: General Purpose Logging

Word Address	Default Value	Bytes	Data Field Type Information
85	70XXH	2	Command set enabled: NOP, READ BUFFER, WRITE BUFFER, volatile write cache enabled/disabled, power management feature set, Security Mode feature set enabled/disabled, SMART feature set enabled/disabled
86	3405H	2	Command set enabled: FLUSH CACHE, FLUSH CACHE EXT, LBA48, CFA feature set, DOWNLOAD MICROCODE
87	4020H	2	Command set/feature default
88	XXXXH	2	UDMA mode, according to-UDMA preformat option
89	0000H	2	Time for Security Erase Unit not specified
90	0000H	2	Time for Enhanced Security Erase Unit not specified
91	0000H	2	Reserved
92	XXXXH	2	Master Password Revision Code
93	XXXXH	2	Hardware Reset Result
94 to 99	0000H	12	Reserved
100 to 103	XXXXH	8	Total number of sectors addressable in LBA48 Mode
104	0000H	2	Reserved
105	0001H	8	Number of sectors per Data Set Management command
106 to 107	0000H	4	Reserved
108 to 111	0000H	8	World Wide Name
112 to 127	0000H	36	Reserved
128	0XXXH	2	Security Status
129	XX00H	2	Write Protect Status. Bit 15 = permanent write protect, out of spare blocks Bit 14 = permanent write protect due to table corruption Bit 13 = read protection due to table corruption Bit 9 = permanent write protect from vendor command Bit 8 = temporary write protect from vendor command
130 to 133	XXXXH	8	Firmware date string

Word Address	Default Value	Bytes	Data Field Type Information
134	848AH	2	General Configuration word for PCMCIA mode (-id1)
135	045AH	2	General Configuration word for True-IDE mode (-id2)
136 to 141	XXXXH	12	Firmware file name
142 to 147	XXXXH	12	Preformat file name
148 to 153	XXXXH	12	Anchor program file name
154 to 159	0000H	12	Reserved
160	A064H	2	CFA Power Mode: no power level 1. Max 100mA
161	0000H	2	Reserved
162	0000H	2	Key Management Schemes: CPRM not supported
163	XXXXH	2	CFA advanced modes: supported and enabled bits
164	XXXXH	2	CFA advanced modes: 80ns I/O and Memory supported. I/O and Memory UDMA modes supported and selected
165 to 168	0000H	8	Reserved
169	0001H	2	Trim bit in Data Set Management supported
170 to 216	0000H	94	Reserved
217	0001H	2	Solid State Device (non-rotating media)
218 to 254	0000H	74	Reserved
255	XXA5H	2	Integrity Word

8.3.2 ID Table Information of PCMCIA Mode

Word Address	Default Value	Bytes	Data Field Type Information
0	848AH	2	General configuration bit-significant information (-id1)
93	0000H	2	Hardware Reset Result not supported

When the “-ide” preformat option has been used, the following words will be different:

Word Address	Default Value	Bytes	Data Field Type Information
83	7401H	2	Command set: FLUSH CACHE, FLUSH CACHE EXT, LBA48, DOWNLOAD MICROCODE
86	3401H	2	Command set enabled: FLUSH CACHE, FLUSH CACHE EXT, LBA48, DOWNLOAD MICROCODE
160 to 164	0000H	10	Reserved

9. Ordering Information

Capacities/Flash type	Standard Temp.	Industrial Temp.
1GB/SLC	RCS001-PH1C	RIS001-PH1C
2GB/SLC	RCS002-PH1C	RIS002-PH1C
4GB/SLC	RCS004-PH1C	RIS004-PH1C
8GB/SLC	RCS008-PH1C	RIS008-PH1C
16GB/SLC	RCS016-PH1C	RIS016-PH1C
32GB/SLC	RCS032-PH1C	RIS032-PH1C
64GB/SLC	RCS064-PH1C	RIS064-PH1C
8GB/MLC	RCM008-PH1C	RIM008-PH1C
16GB/MLC	RCM016-PH1C	RIM016-PH1C
32GB/MLC	RCM032-PH1C	RIM032-PH1C
64GB/MLC	RCM064-PH1C	RIM064-PH1C
128GB/MLC	RCM128-PH1C	RIM128-PH1C

10. Product Part Number Naming Rule